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Abstract
Statistical carry lookahead adder（SCLA） is a Self-time adder that proposed in 1996. It’s regard 4Bit as one block, so it will send a completed message to notice the next stage after operation, and it would change the operation time follow the different message input. It has a good extensible, because it has regard 4Bit as one block.
SCLA is not easy to design, because it complete it’s message is produce by match delay. This way is to produce the corresponding completion signal according to the time for operation by match delay. Until 1999, somebody to bring up an idea, we can use Manchester carry chain(MCC) to be the sand on delay of complete message. Although it solve the problem of design on the surface but actually have the same problem as the original one. When the circuit has not complete operation yet, the signal advance of postpones time are not enough, thus will make mistake of the next stage. Moreover the new structure still takes out of the new problem.
This paper to bring up some new architecture, directed on SCLA architecture. Not only can improve the problem of postpones time are not enough to make advance to send, but also can raise the speed of an operation. In addition, it can match the original architecture according to the demand, use alternatively.
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